THE INVENTION CLAIMED IS:

1. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a silicide on the source/drain junctions and on the gate,

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming contact liners in the contact holes; and

forming contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

2. The method as claimed in claim 1 wherein:

forming the tungsten nitride contact liners uses an atomic layer deposition process.

3. The method as claimed in claim 1 wherein:

forming the contact liners forms at a temperature of less than or equal to about the thermal budget for the silicide.

4. The method as claimed in claim 1 wherein:

forming the silicide forms a nickel silicide.

5. The method as claimed in claim 1 wherein:

forming the contacts forms a tungsten material; and

forming the contact liners forms a tungsten nitride material.

6. A method of forming an integrated circuit comprising:

providing a semiconductor substrate;

forming a gate dielectric on the semiconductor substrate;

forming a gate on the gate dielectric;

forming source/drain junctions in the semiconductor substrate;

forming a nickel silicide on the source/drain junctions and on the gate,

depositing an interlayer dielectric having contact holes therein above the semiconductor substrate;

forming tungsten nitride contact liners in the contact holes; and

forming tungsten contacts in the contact holes over the contact liners.

7. The method as claimed in claim 6 wherein:

forming the tungsten nitride contact liners uses an atomic layer deposition process.

8. The method as claimed in claim 6 wherein:

forming the tungsten nitride contact liners forms at a temperature of less than or equal to about 400 degrees centigrade.

9. The method as claimed in claim 6 wherein:

forming the nickel silicide uses an ultra-thin thickness of a nickel silicide metal.

10. The method as claimed in claim 6 wherein:

depositing the interlayer dielectric deposits a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

11. An integrated circuit comprising:

a semiconductor substrate;

a gate dielectric on the semiconductor substrate;

a gate on the gate dielectric;

source/drain junctions in the semiconductor substrate;

a silicide on the source/drain junctions and on the gate,

an interlayer dielectric having contact holes therein above the semiconductor substrate;

contact liners in the contact holes; and

contacts in the contact holes over the contact liners, whereby the contact liners are formed of a nitride of the material of the contacts.

12. The integrated circuit as claimed in claim 11 wherein:

the silicide is a nickel silicide.

13. The integrated circuit as claimed in claim 11 wherein:

the silicide is an ultra-thin nickel silicide.

14. The integrated circuit as claimed in claim 11 wherein:
the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

15. The integrated circuit as claimed in claim 11 wherein:
the contacts in the contact holes are materials selected from a group consisting of tantalum, titanium, tungsten, copper, gold, silver, an alloy thereof, a compound thereof, and a combination thereof.

16. The integrated circuit as claimed in claim 11 wherein:
the contacts are a tungsten material; and
the contact liners are a tungsten nitride material.

17. An integrated circuit comprising:
a semiconductor substrate;
a gate dielectric on the semiconductor substrate;
a gate on the gate dielectric;
source/drain junctions in the semiconductor substrate;
a nickel silicide on the source/drain junctions and on the gate,
an interlayer dielectric having contact holes therein above the semiconductor substrate;
tungsten nitride contact liners in the contact holes; and
tungsten contacts in the contact holes over the contact liners.

18. The integrated circuit as claimed in claim 17 wherein:
the nickel silicide is an ultra-thin thickness of a nickel silicide material.

19. The integrated circuit as claimed in claim 17 wherein:
the interlayer dielectric is a dielectric material having a dielectric constant selected from a group consisting of medium, low, and ultra-low dielectric constants.

20. The integrated circuit as claimed in claim 17 wherein:
the nickel silicide further comprises arsenic doping.